Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**G**

**SOURCE**

**.043”**

**.074”**

**Top Material: Al**

**Backside Material: TiNiAg**

**GATE Size: .006” X .007”**

**Backside Potential: DRAIN**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .043” X .074” DATE: 4/25/22**

**MFG: FAIRCHILD THICKNESS .008” P/N: FDT434P**

**DG 10.1.2**

#### Rev B, 7/1